

IPC-2517A

Sectional Requirements for Implementation of Assembly In-Circuit Testing Data Description [ASEMT]

“The data model of this standard shall be in effect until 2001-12.” At that time, the committee will consider changes, revision, other actions.

IPC-2517A

November 2000

A standard developed by IPC

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Adopted October 6. 1998

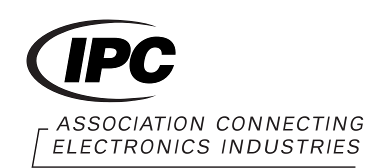
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IPC-2517A



[ASEMT]

Sectional Requirements for Implementation of Assembly In-Circuit Testing Data Description

A standard developed by the Computerized Data Format Standardization Subcommittee (2-11) of the Data Generation and Transfer Committee (2-10) of the Institute for Interconnecting and Packaging Electronic Circuits.

The GenCAM format is intended to provide CAD-to-CAM, or CAM-to-CAM data transfer rules and parameters related to manufacturing printed boards and printed board assemblies. The requirements of IPC-2511 are a mandatory part of this sectional standard.

This standard is part of the GenCAM 1.5 release.

> **"The data model of this standard shall be in effect until 2001-12."** At that time, the committee will consider changes, revision, other actions.

Users of this standard are encouraged to participate in the development of future revisions.

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Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC Data Generation and Transfer Committee of the IPC Data Transfer Solution DTS Subcommittee are shown below, it is not possible to include all of those who assisted in the evolution of this standard. To each of them, the members of the IPC extend their gratitude.

Data Generation and Transfer Committee

Chairman
Harry Parkinson
Digital Equipment

Data Transfer Solution DTS Subcommittee

Chairman
Harry Parkinson
Digital Equipment

Technical Liaisons of the IPC Board of Directors

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Beaver Brook Circuits Inc.

Special Note of Thanks

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Sectional Requirements for Implementation of Assembly In-Circuit Test Data Description (ASEMT)

1 SCOPE

This standard specifies data formats used to describe printed board assembly in-circuit testing methodologies. These formats may be used for transmitting information between printed board designers, board fabricators, and assembly manufacturers. The formats are also useful when the manufacturing cycle includes computer-aided processes and numerical control machines.

The information can be used for both manual and for digital interpretation. The data may be defined in either English or SI units.

1.1 Interpretation

"Shall", the emphatic form of the verb, is used through this standard whenever a requirement is intended to express a provision that is mandatory. Deviation from a shall requirement is not permitted, the compliance test modules (CTMs) developed to check syntax, semantics and completeness, will prompt the user to correct the ambiguity, or to insert missing information.

1.2 Assembly In-Circuit Test Focus

The GenCAM format requirements are provided in a series of standards focused on printed board manufacturing, assembly, inspection, and testing. Thisstandard (IPC-2517) provides information on assembly in-circuit test requirements. The generic standard (IPC-2511) contains general requirements and is a mandatory part of the requirements of this standard, and provides general information necessary to completely understand the GenCAM structure.

2 APPLICABLE DOCUMENTS

The following documents contain provisions which, through references in the text, constitutes provisions of IPC-2517. At the time of publication, the additions indicated were valid. All documents are subject to revision and parties to agreements based on this generic standard are encouraged to investigate the possibility of applying the most recent additions of the documents indicated below.

IPC-T-50		Terms and Definitions for Interconnecting and Packaging Electronic Circuits
IPC-2511	(MANGN)	Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer
IPC-2512	(ADMIN)	Sectional Requirements for Implementation of Administrative Methods for Manufacturing Data Description
IPC-2513	(DRAWG)	Sectional Requirements for Implementation of Drawing Methods for Manufacturing Data Description
IPC-2514	(BDFAB)	Sectional Requirements for Implementation of Printed Board Fabrication Data Description.
IPC-2515	(BDTST)	Sectional Requirements for Implementation of Bare Board Product

		Electrical Testing Data Description
IPC-2516	(BDASM)	Sectional Requirements for Implementation of Assembled Board Product Manufacturing Data Description
IPC-2518	(PTLST)	Sectional Requirements for Implementation of Part List Product Data Description
IPC-2519	(MODEL)	Sectional Requirements for Information Model Data Related to the Printed Board and Printed Board Manufacturing Descriptions.

3 REQUIREMENTS

The requirements of IPC-2511 are a mandatory part of the standard. The IPC-2511 document describes the generic requirements of the GenCAM format. The format specifies details specifically for information interchange of data related to printed board manufacturing, assembly, and test.

GenCAM is comprised of twenty sections as described in the generic GenCAM standard, IPC-2511. The sections are shown in Tables 3-1 and 3-2 of the IPC-2511.

Each section has a specific function or task respectively and is independent of each other. Accordingly, the information interchange for a specific purpose is possible only if the sections required for such a purpose have been prepared.

3.1 Categories and Content

Table 3-1 (below) provides the section names that are appropriate for the printed board assembly testing process. The letter **"M"** signifies a mandatory requirement. The letter **"O"** signifies an optional characteristic that may or may not be pertinent to the particular file. A dash signifies an extraneous section (unnecessary); CTMs will not reject file summaries if extraneous sections are present.

The table signifies two requirement conditions separated by a "/". The first representation of requirements is intended to convey those GenCAM sections that **shall** be available as the initial input to the Assembly processes. The second instance of a requirement is to signify those data that **shall** be available once the processing descriptions have been completed.

Table 3-1 GenCAM Section Relationahips for Assembled Board Test

Section Identifiers	Assembly Test Program Generation	Assembly Test Fixture Generation
HEADER	M/M	M/M
ADMINISTRATION	M/M	M/M
PRIMITIVES	M/M	M/M
ARTWORKS	M/M	M/M
LAYERS	M/M	M/M
PADSTACKS	M/M	M/M
PATTERNS	M/M	M/M
PACKAGES	M/M	M/M
FAMILIES	M/M	-/-
DEVICES	M/M	M/M
MECHANICALS	M/M	M/M
COMPONENTS	M/M	M/M

Section Identifiers	Assembly Test Program Generation	Assembly Test Fixture Generation
ROUTES	M/M	M/M
POWER	M/M	M/M
TESTCONNECTS	O/O	O/M
BOARDS	M/M	M/M
PANELS	O/O	O/O
FIXTURES	-/O	O/M
DRAWINGS	M/M	M/M
CHANGES	-/O*	-/O*

* The CHANGES section is used independently to alter previously sent files. Included **shall** be a HEADER section (for revision status and identification) and an ADMINISTRATION section to show effectivity

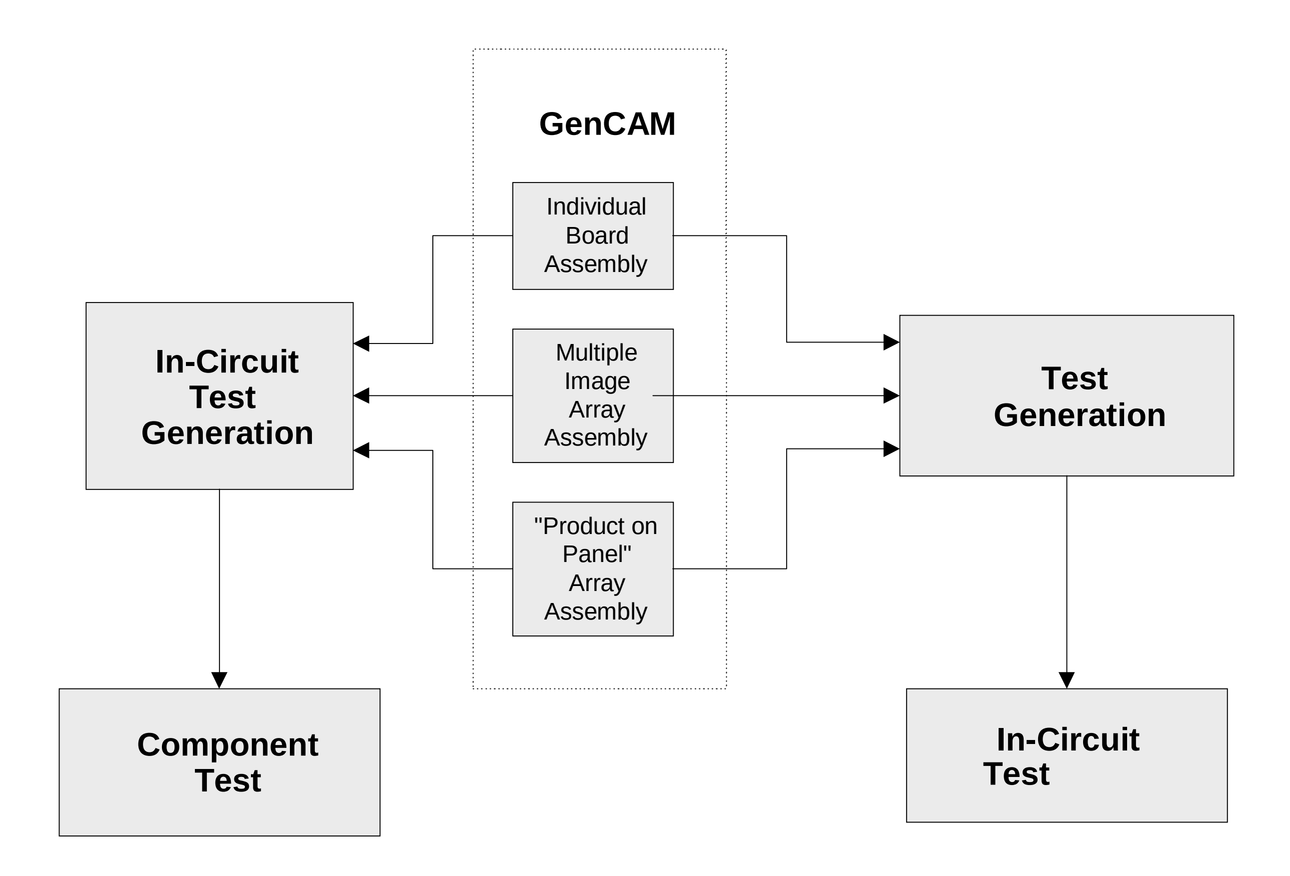


Figure 3-1 In-Circuit Test and Fixture Generation Activities

3.2 Assembled In-Circuit Test

This document is intended to enumerate and explain the data requirements of the assembled board, in-circuit test step of the electronic circuit board manufacturing process. Data needs are described in the context in which they are used, and where assumptions are made, an attempt has been made to explain them. The overall effort is meant to identify and categorize data, to a reasonably, but vendor independent level. Not all data will be applicable to all situations, but any data that may be required should be listed and be provided with a syntax and location within the standard's data sets.

3.2.1 Fundamental Assumptions

In-circuit test is understood to be the setup and application of a stimulus and a subsequent comparison of an expected response to a recorded response, each of which have properties such as voltage, current, frequency and time increment.

In-circuit test is typically performed in three sequenced stages.

- **Shorts Test** - This is a d.c. resistance measurement involving voltage and current levels sufficiently small that the P/N-junctions of semiconductor components are not turned-on. It is performed before power is applied to the assembly to assure that no damage is incurred at power-up. This test is different from bare board test because of the properties of the devices that now populate the board. Knowledge of the open/closed state of switches, jumpers and fuses is needed, along with knowledge of components such as potentiometers whose quiescent state can provide a low d.c. resistance path between circuit nets, and capacitive and inductive components which initially appear as current sinks.

- **Unpowered Tests -** These are typically differential measurement tests of analog components.

- **Powered Tests -** As the name implies, these are tests performed while power is applied to the board, typically on digital or mixed signal components or component clusters.

Functional testing specifications are not included in the standard.

3.2.2 Assembly Identification Requirements

The first of the identification requirements is the overall assembly identifier for the coupon, board, or panel. This is typically an internal part number, product model or product family and is most often based on bare board artwork. In addition there is often an assembly revision identifier to denote the generation of the artwork. If the assembly is a panel of homogeneous or heterogeneous (product-on-panel) subassemblies, then it is important that the super-assembly identifier be differentiated from those of the subassemblies to prevent confusion, as is the case when individual boards are broken out for repair and then re-tested.

Revisions of a board should not be confused with versions of a board. In the latter case a single bare-board revision may be the basis of multiple products whose differences are in component type, component nominal value, ROM/BIOS/PLD loads, or in the presence or absence of components. Each version of the assembly must be uniquely identifiable.

3.2.3 Topology - Logical Circuit Description

In general, an electronic assembly can be described from one of two viewpoints. From the component-major view each component designator is listed with the mapping between the pins and their associated net. In the net-major description, each signal name is listed along with its associated component-pin locations and via/pad access. Both views must be derivable from the GenCAM file.

3.2.4 Components

The description of the assembled PCB must be capable of capturing and conveying both its electrical connectivity and its physical properties. Of primary importance is the component type, and for analog measurements, their nominal value and the allowable deviation from the nominal, typically expressed as a +/- tolerance percentage. Though many passive components (i.e. resistors, inductors) can be tested without regard to their orientation in the circuit, that is not true of such as diodes and electrolytic capacitors. The association of the pin-polarity must be communicated for these.

Note also that there may not be a 1-to-1 correspondence between the components that are tested, and the packages that are mounted, and therefore replaceable (e.g. resistor networks). The package hierarchy that maps between component tests and replaceable package becomes an important element in the description language, for test and repair.

Most board assemblers have internal part numbers to identify the devices which make up the assembly, but often one internal part number maps to many manufacturer's part numbers when the parameters of the devices are sufficiently similar as to make them interchangeable. It is important that Test be provided the manufacturer's part number to identify other, potentially significant differences (e.g. pin-outs, geometry, and package type). For Boundary Scan (IEEE-1149.1) compliant devices, the manufacturer's part number denotes the BSDL file with its mapping of device-pins to test access port (TAP) signals.

From the package type can be determined thermal characteristics of the device. Where back-driving (overdriving) is used for in-circuit test of digital or mixed signal devices, it is necessary to calculate the time duration and level for the electrical current to prevent damage to the device, based on insight into the heat dissipation characteristics of the part. This will dictate the order in which components or component clusters are tested. Package type can also be a determining factor when selecting the depth to set the probe receptacles and also in choosing the type of probe tip.

The logic family (TTL, CMOS etc.) of the device, and for dual-family devices, the family of each pin of the device, is information which is needed to determine the tester resources assignment to the associated net. Also needed for this task is the signal type of the devices at a pin level. These will include the designation of the fixed, power and ground pins, the clock pins, and the enable/disable pins, as well as those driven as inputs, received as outputs, or both (bi-directional).

3.2.5 Nets

It is also important to maintain data on the circuit nets themselves. There are two basic net categories: signal nets (drive-able) and fixed nets (non-drive-able). Signal nets can be further described as normal or high-speed signal nets. It is also important to provide the ability to describe logical net groups, where matched impedance paths are critical to signal integrity.

Fixed nets include not only those to which external power is applied during powered test, but also those nets to which power may be supplied or derived on the board. In the case of the former, Test must know the voltage level and polarity as well as the current limit and the voltage reference net, typically board ground.

3.2.6 Physical Descriptions

Besides the parametric data and logical connectivity that is described above, there is the category of physical data that is necessary for in-circuit test. Though some of this information is used in generating the tests, it is most often associating with fixturing and probing the assembly. The first of this type of data describes the outline points of the coupon, panel or board. This is typically defined as a series of vertices and/or arcs that describe a closed, or close-able polygon relative to an origin point either within or outside of the assembly itself. In the case of a panel, there is the subsequent definition of the polygon of each subassembly along with their offset and rotation relative to the panel origin. In order to maintain probe alignment, it is necessary to define the fiducial or tooling pin locations for each assembly/subassembly relative to their own origin. Also relative to this origin is each of the unmasked, potentially probing locations of the assembly. Though each of these (X,Y) locations can be named (typically based on a device-pin) or un-named, they must each maintain their association to a logical signal of the assembly. These locations must also be allowed to carry attributes of accessibility and probable surface or direction. A minimum set of accessibility attributes includes mandatory, manual-only (or flying probe), and inaccessible, while the surface must encompass at least top and/or bottom side probability.

As new techniques and new probe technologies have been advanced, device geometry has become increasingly important. The assembly side on which a device is mounted, along with its footprint, are necessary for probing accuracy with capacitive and inductive coupling techniques for determining pin connectivity. This information is also used in placing supports, drilling and routing and is fundamental for aiding in device location at repair.

Though digital test vector definition is beyond the scope of this standard, there is need for the ability to communicate many attributes that are part-name specific. Package type, logic family and pin signal categories are the most important of these.

Finally, there is information pertaining specifically to the fixturing of the assembly. Test Engineering or manufacturing may wish to communicate the type of fixture to be built (e.g. vacuum, pneumatic, mechanical actuation; single well, dual-well) and it’s wiring method (manual, automatic, wireless). Test probing locations and specifications are a necessary part of the data set, thought they may be an input to assembled board test, or may be a product thereof. Many other fixturing parameters are possible, though most are ICT system manufacturer specific.

4 GENERAL RULES

The following details reflect the rules in GenCAM to meet the requirements for in-circuit test of assembled boards. These rules are intended to meet the needs of the testing entity to understand the customer requirements.

Wherever necessary, additional requirements have been detailed to reflect precision. The attributes and rules for GenCAM described in IPC-2511 are referenced.

Wherever necessary, detailed descriptions or definitions of entries, attributes or characteristics are described according to the following issues detailed in Tables 4-1 and 4-2 and descriptions. See Figure 4-1 for an example of the in-circuit test process and data flow.

Table 4-1 Assembled Board Test - Keyword Usage

Need Identifier	Section Keyword	Keyword Usage
Assembly Identifier Assembly Revision Identifier Assembly Load Variant Identifier Board Identifier Board Revision Identifier Panel Identifier Panel Revision Identifier	HEADER	ASSEMBLY.<assembly_name> ASSEMBLY.<assembly_revision> ASSEMBLY.<assembly_number> BOARD.<board_name> BOARD.<board_revision> PANEL.<panel_name> PANEL.<panel_revision>
Fixture identifier Fixture application	FIXTURES	FIXTURE.<fixture_ref> FIXTURE.<fixture_app> FIXTURE.<fixture_function>
Panel Footprint Board Footprint	PANELS BOARDS	PANEL.<panel_ref> PANEL.OUTLINE BOARD.<board_ref> BOARD.OUTLINE
Board location in a panel	PANELS	PANEL.PLACEMENT.<product_ref> PANEL.PLACEMENT.<place>
Board/Panel placement on a fixture	FIXTURES	FIXTURE.PLACEMENT.<product_ref> FIXTURE.PLACEMENT.<place>
Board Keepout Areas Panel Keepout Areas Fixture Keepout Areas	BOARDS PANELS FIXTURES	BOARD.KEEPOUT.<closed_shape> PANEL.KEEPOUT.<closed_Shape> FIXTURE.KEEPOUT.<closed_shape>
Designer, Engineer, Billing Address	ADMINISTRATION	DESIGNER.<person_ref> ENGINEER.<person_ref> BILLTO.<person_ref>
Units of Measure	HEADER	UNITS.<dimension>,[<grid_value>] ANGLEUNITS.<angular_unit>
Board Schematics, Surrounding Circuitry, Part Locator	DRAWINGS	DRAWING.<drawing_type>
Component Reference Designator	COMPONENTS	COMPONENT.<ref_desig>
Mfg. Part Number – Library Model	COMPONENTS DEVICES	COMPONENT.DEVICEREF.<part_ref> DEVICE.<part_name> DEVICE.PART.<enterprise_part_id> DEVICE.ALIAS.<enterprise_part_id>
Device Logic Family Options: Drive High, Drive Low Receive High, Receive Low Edge Speed Open Input Default Load	FAMILIES	FAMILY.<drive_high> FAMILY.<drive_low> FAMILY.<receive_high> FAMILY.<receive_low> FAMILY.<open_input_logic> FAMILY.<edge_speed> FAMILY.<load>
Component - Logical Description Component Logic Family	COMPONENTS DEVICES FAMILIES	COMPONENT.<device_ref> DEVICE.<family_ref> FAMILY.<family_name>
Component package type and physical description	COMPONENTS DEVICES PACKAGES	COMPONENT.<device_ref> DEVICE.<package_ref> PACKAGE.<package_name> PACKAGE.<type> PACKAGE.BODY.<artwork_ref> PACKAGE.<height> PACKAGE.<standoff>
Component locations	COMPONENTS DEVICES LAYERS	COMPONENT.<place> COMPONENT.<device_ref> DEVICE.<package_ref> PACKAGE.<centroid> COMPONENT.<layersingle_ref> LAYERSINGLE.<layer_name>

Need Identifier	Section Keyword	Keyword Usage
Component values and tolerances	COMPONENTS DEVICES	COMPONENT.DEVICEREF.<part_ref>, DEVICE.VALUE (VALUE, TOL, NTOL, PTOL are fixed field parameters)
Signal names & characteristics	ROUTES	ROUTE.<net_name>
Component-pin to net name association	ROUTES COMPONENTS	ROUTE.<net_name> ROUTE.COMPPIN,.<component_ref>
Power net(s), reference net(s) voltage, current-limit	POWER	SUPPLY.<voltage> SUPPLY.<current_limit>
Signal potential probing locations and access attributes	ROUTES	ROUTE.VIA.<testpoint_xy> ROUTE.VIA.<access_desc> ROUTE.TESTPAD.<testpoint_xy> ROUTE.TESTPAD.<access_desc> ROUTE.COMPPIN.<testpoint_xy> ROUTE.COMPPIN.<access_desc> ROUTE.CONNPIN.<testpoint_xy> ROUTE.CONNPIN.<access_desc>
Component Test Failure/Debug Message	COMPONENTS	COMPONENT., ONFAIL.<text>
Test point, probe size, probe receptacle depth, probe spring-force, probe tip	TESTCONNECTS	TESTPROBE.<offset> TESTPROBE.<probe_size> TESTPROBE.<recepticle_depth> TESTPROBE.<tip_type>
Tester resource pin	TESTCONNECTS	TESTPIN.<testpin_name> TESTCONNECT.TESTPINREF.<testpin_ref>
Test fixture electronics connection	TESTCONNECTS	FIXELEC.<fixelec_signal_name> TESTCONNECT.FIXELECREF.<fixelec_signal_ref>
Special wiring group and wiring type	TESTCONNECTS	TESTCONNECT.<bunch_type> TESTCONNECT.<bunch_label>
Engineering Change Effects Corrections To Previously Sent Data	CHANGES	CHANGE.ADD CHANGE.DELETE CHANGE.REPLACE CHANGE.RENAME CHANGE.ADDPRODUCT CHANGE.DELETEPRODUCT CHANGE.RENAMEPRODUCT

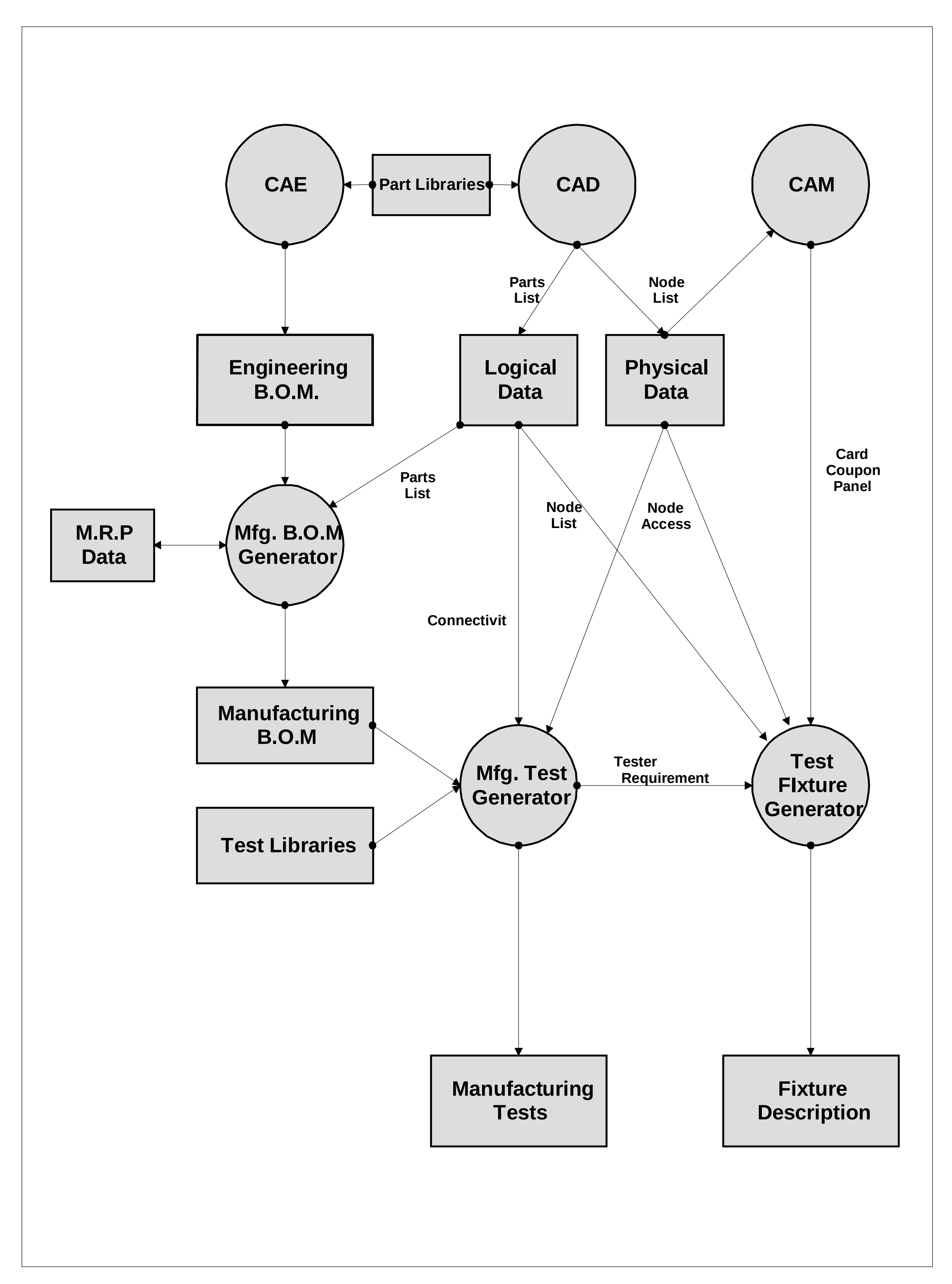


Figure 4-1 Assembled Board In-Circuit Test - Processes and Data Flow

5 MODELING

The data files of GenCAM may be mapped to the information models. Information models are developed to ensure that complete mapping is capable between the information provided within the GenCAM characteristics. The correlation is provided in the activity models shown in IPC-2519.

All data activities are based on activity models as defined in IPC-2519. The activity models covered by CAD and CAM include the engineering, design, administrative, and fabrication and assembly characteristics. Each of these sections are intended to be detailed into various levels of activity much like layers of information needed to perform a particular manufacturing process.

Figure 5-1 shows the activity needed to develop administrative data.

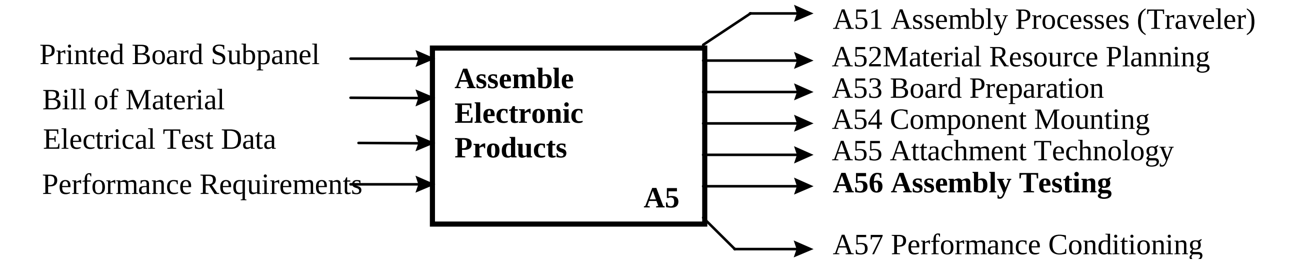


Figure 5-1 In-Circuit Test Data Activity Models

5.1 Information Models

Information models are also helpful in understanding the requirements of the assembly in-circuit test section. Attribute information is correlated to the parameters of GenCAM as well as to the activity models used to describe assembly in-circuit test data.

EXPRESS is an international information modeling format supported by ISO 10303-11. The graphic representation of EXPRESS is known as EXPRESS-G. Appendix A provides an explanation of the different EXPRESS-G requirements. Figures 5-2 through 5-5 show the EXPRESS-G version of the GenCAM FAMILIES, TESTCONNECTS, POWER, and FIXTURES sections. See www.gencam.org for complete EXPRESS-G model.

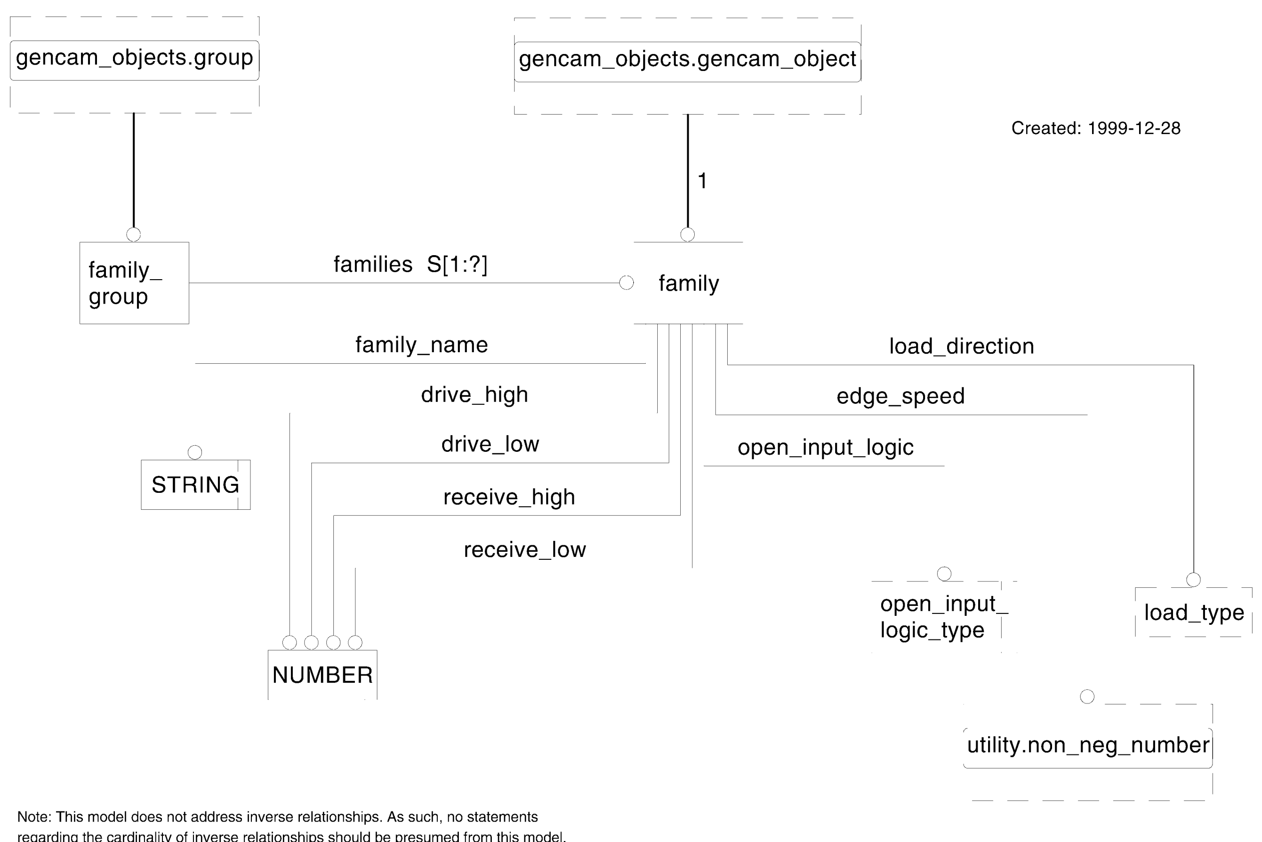


Figure 5-2 EXPRESS-G for FAMILIES

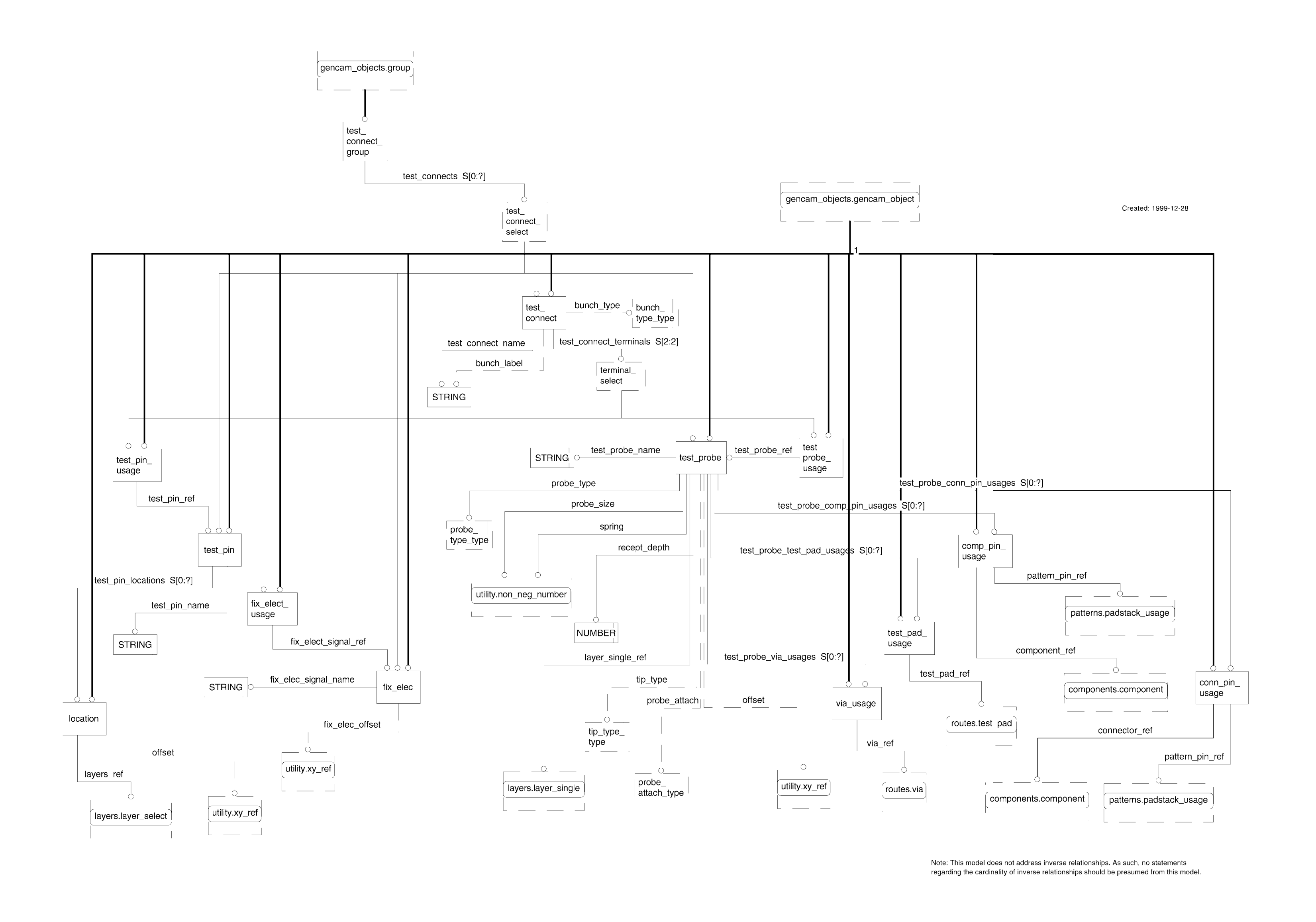
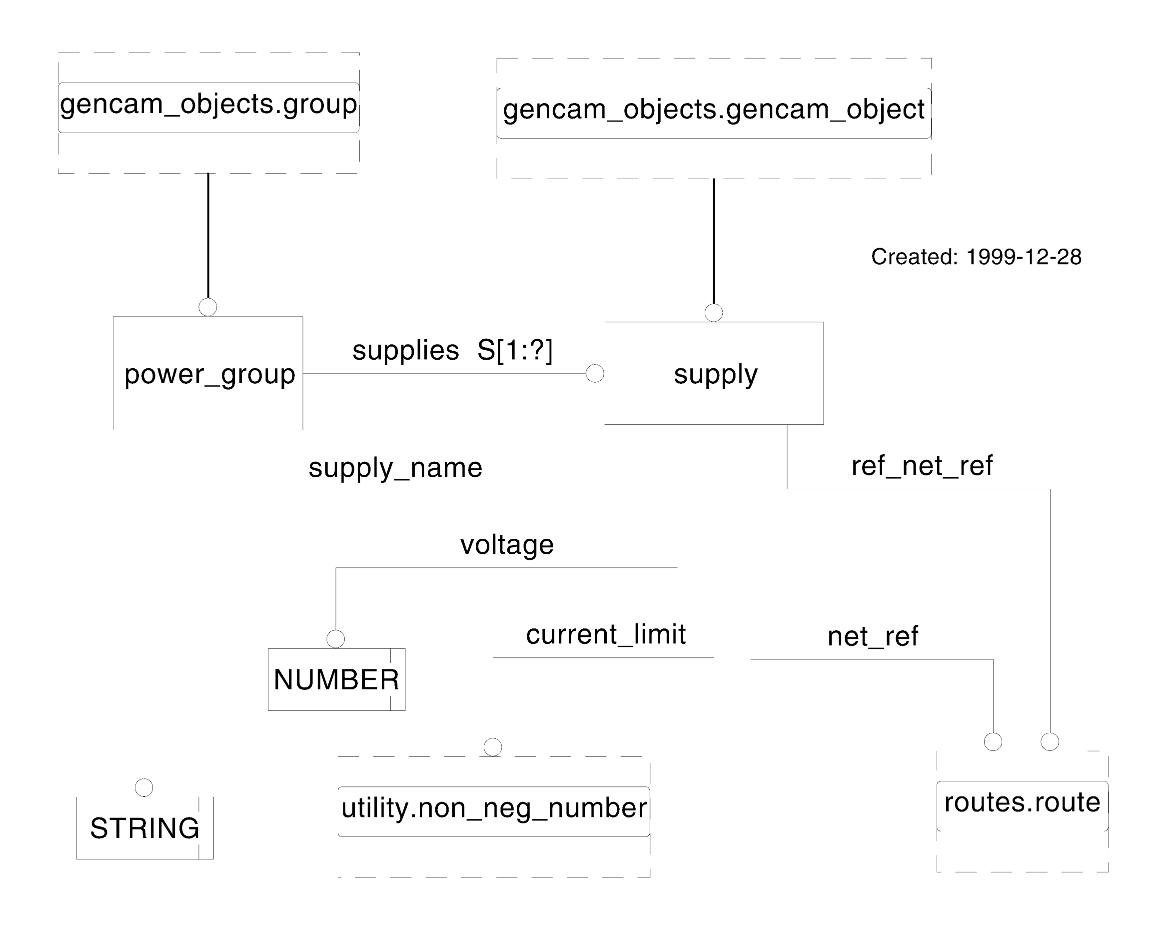


Figure 5-3 EXPRESS-G for TESTCONNECTS



Note: This model does not address inverse relationships. As such, no statements regarding the cardinality of inverse relationships should be presumed from this model.

Figure 5-4 EXPRESS-G for POWER

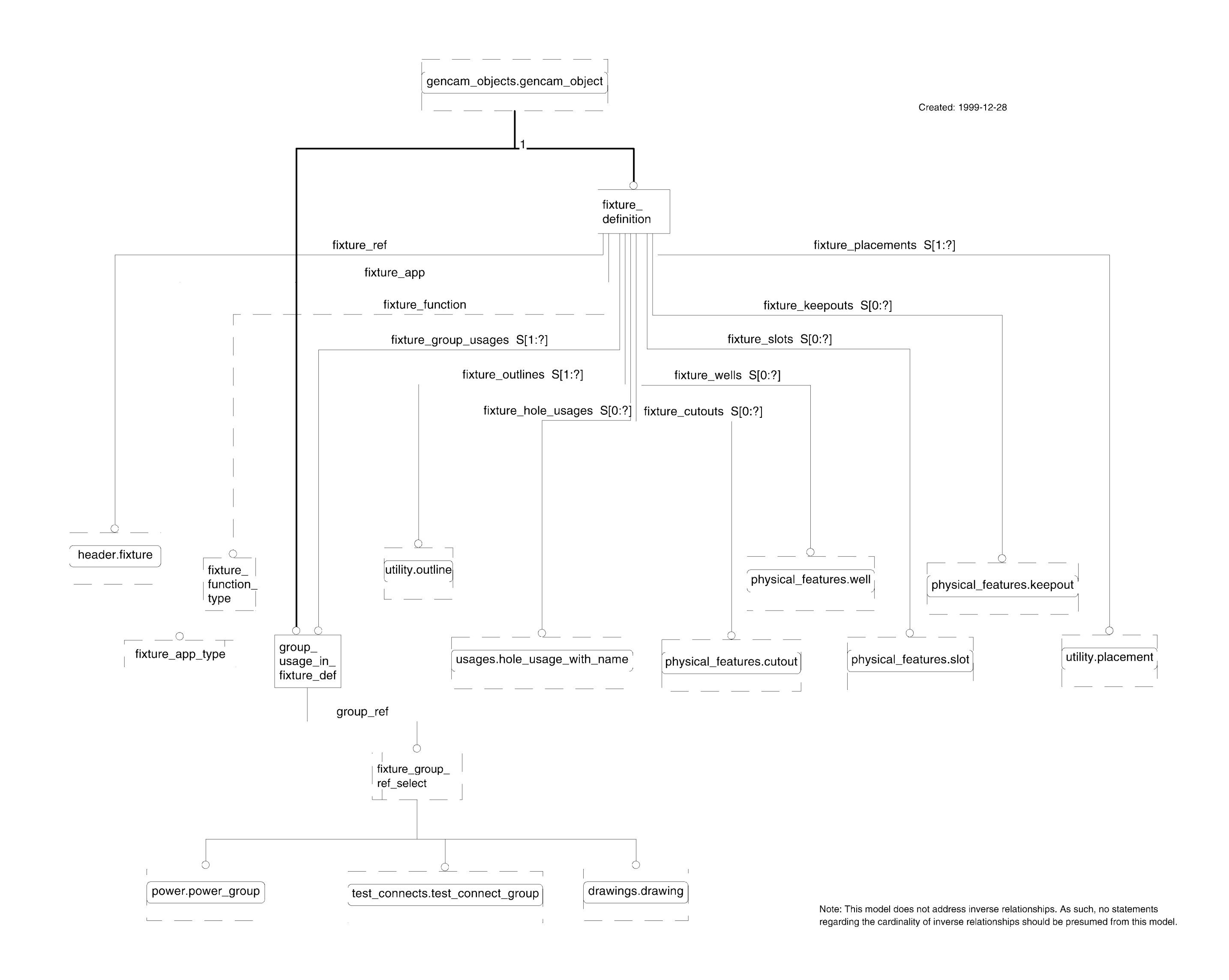


Figure 5-5 EXPRESS-G for FIXTURES

6 REPORT GENERATORS

Data can be extracted from GenCAM files to produce various formats that are commonly used in the electronics industry. The types of reformatting can be used for electronic data transfer to tools or to facilitate inspection and human interpretation of text and/or graphic rendering. Note that no extraction tools are included in the IPC-2510 standard. Their creation is left to the industry as the need arises.

The following figures show examples of assembled board test fixturing extractions.

```
--------------------------------------------------------------------------
3070 FIXTURE INSERTION REPORT
/users/user1/VBoard/fixture/inserts
------------------------------------------------------------------------------
Insertion Method : Automatic
-----------------------------------------------------------------------------
(bank row col )     X       Y     Type   Spring Net  Name  On Device
---------------|---------------|--------|------|----------|------------------
[2 17.25  69.6]   32236  -32057 100 mil   8 oz    R203-2   r203.2
[2 17.25  63.6]   41236  -32057 100 mil   8 oz    R206-2   r206.2
[2 17.25  57.6]   50236  -32057 100 mil   8 oz    R210-2   r210.2
[2 17.25  51.6]   59236  -32057 100 mil   8 oz    R213-2   r213.2
[2 17.27  22.8]  102366  -32197 100 mil   8 oz     GND     u304.8
[2 17.27  20.8]  105366  -32197 100 mil   8 oz   CARRYOUT  u304.9
[2 17.27  06.8]  126366  -32197 100 mil   8 oz     GND     r315.2
[2 16.42  13.5]  116366  -26197 100 mil   8 oz    R315-1   sw302.1
[2 16.99  13.5]  116366  -30197 100 mil   8 oz   SW302-3   sw302.3
[2 16.13  17.5]  110366  -24197 100 mil   8 oz     GND     cb312.2
[2 16.56  20.8]  105366  -27197 100 mil   8 oz     ADD6    u304.14
[2 16.70  20.8]  105366  -28197 100 mil   8 oz      S6     u304.13
[2 16.85  20.8]  105366  -29197 100 mil   8 oz     ADD7    u304.12
[2 16.27  22.8]  102366  -25197 100 mil   8 oz      S5     u304.1
[2 16.56  22.8]  102366  -27197 100 mil   8 oz     ADD5    u304.3
[2 16.70  22.8]  102366  -28197 100 mil   8 oz      S4     u304.4
[2 16.85  22.8]  102366  -29197 100 mil   8 oz     ADD4    u304.5
[2 16.42  38.8]   78366  -26197 100 mil   8 oz     GND     ac307.2
[2 16.85  39.5]   77366  -29197 100 mil   8 oz     GND     ar309.2
[2 16.85  49.8]   61916  -29197 100 mil   8 oz    R212-2   r212.2
[2 16.13  50.8]   60366  -24197 100 mil   8 oz   QF201-D   qf201.D
[2 16.85  53.5]   56366  -29197 100 mil   8 oz    R212-1   r213.1
[2 16.85  55.8]   52916  -29197 100 mil   8 oz    R209-2   r209.2
[2 16.85  58.5]   48916  -29197  75 mil   8 oz    R209-1   r209.1
[2 16.85  61.8]   43916  -29197  75 mil   8 oz    R205-2   r205.2
[2 16.85  65.5]   38366  -29197  75 mil   8 oz    R205-1   r206.1
[2 16.13  66.8]   36366  -24197  50 mil   4 oz    L201-2   l201.2
[2 16.85  67.8]   34916  -29197  50 mil   4 oz    R202-2   r202.2
[2 13.85  31.5]   89366   -8197 100 mil   4 oz     GND     cb301.2
[2 13.99  31.5]   89366   -9197 100 mil   4 oz     GND     cb307.2
(2 23.00  64.0)   40611   72275   Pin             R213-2
(2 23.00  63.0)   42111   72275   Pin             R206-2
(2 23.00  62.0)   43611   72275   Pin             R209-1
(2 23.00  61.0)   45111   72275   Pin             R209-1
(2 23.00  60.0)   46611   72275   Pin              GND
(2 23.00  59.0)   48111   72275   Pin              GND
(2 23.00  44.0)   70611   72275   Pin             R210-2
(2 23.00  43.0)   72111   72275   Pin             R212-1
```

```
(2 23.00  42.0)   73611   72275   Pin              R213-2
(2 23.00  40.0)   76611   72275   Pin               GND
(2 23.00  39.0)   78111   72275   Pin               GND
(2 23.00  24.0)  100611   72275   Pin              R210-2
(2 22.84  76.4)   21986  -71177 Tooling
(2 06.42  02.5)  132896   43773 Tooling
```

Figure 6-1 Assigned Fixture Hardware Inserts

```
M47,EXCELLON,Version,2
M47,X+Y+
M47,MODE:
M47,Absolute,X,Y
M47,Leading,Zeros
M47,Trailing,Zeros
M47,Inch
M47,T01,=,100,Mil,Ctr
M47,Probe,Sockets
M47,1.75mm,Long,Flute
M47,T04,=,Scanner,Pin
M47,2.25mm,Long,Flute
M47,T05,=,Tooling,Pin
M47,3.60mm,Std.,Flute
T01
X-03.2057Y+03.2236
X-03.2057Y+04.1236
X-03.2057Y+05.0236
X-03.2057Y+05.9236
X-03.2197Y+10.2366
X-03.2197Y+10.5366
X-03.2197Y+12.6366
X-02.6197Y+11.6366
X-03.0197Y+11.6366
X-02.4197Y+11.0366
X-02.7197Y+10.5366
X-02.8197Y+10.5366
X-02.9197Y+10.5366
X-02.5197Y+10.2366
X-02.7197Y+10.2366
X-02.8197Y+10.2366
X-02.9197Y+10.2366
X-02.6197Y+07.8366
X-00.8197Y+13.1366
X-00.9197Y+13.1366
T04
X-07.2275Y+04.0611
X-07.2275Y+04.2111
X-07.2275Y+04.3611
X-07.2275Y+04.5111
X-07.2275Y+04.6611
X-07.2275Y+04.8111
X-07.2275Y+07.0611
T05
X-07.1177Y+02.1986
X+04.3773Y+13.2896
T01
M47,Blind,Holes
X-03.2057Y+03.3586
X-03.2057Y+04.2586
```

```
X-03.2057Y+05.1586
X-03.2057Y+06.0586
X-03.1197Y+10.2366
X-03.2197Y+12.1366
X-02.8197Y+11.6366
X-02.4197Y+10.6366
```

Figure 6-2 Fixture Probe Plate Drill File

```
-----------------------------------------------------------------------------
3070 FIXTURE WIRING REPORT
/users/user1/VBoard/fixture/wires
-----------------------------------------------------------------------------
Wiring Method: Simi-Automatic
Length Ga Color |From|(bank row col )|#| To  |(bank row col )|#|On Device
------|--|------|----|---------------|-|-----|---------------|-|--------------
   1.5 28 Black  Pin  (2 14.00  39.0) 1 Probe [2 13.99  31.5] 1 cb307.2
   5.0 28 Black  Pin  (2 16.11  60.0) 1 Probe [2 13.99  31.5] 2 cb307.2
   6.5 28 Black  Pin  (2 20.00  60.0) 1 Probe [2 13.99  31.5] 3 cb307.2
   3.5 28 Black  Pin  (2 13.00  50.0) 1 Probe [2 13.85  31.5] 1 cb301.2
   5.0 28 Black  Pin  (2 16.11  59.0) 1 Probe [2 13.85  31.5] 2 cb301.2
   6.5 28 Black  Pin  (2 20.00  59.0) 1 Probe [2 13.85  31.5] 3 cb301.2
   3.5 28 Black  Pin  (2 16.00  40.0) 1 Probe [2 13.99  24.2] 1 cb308.2
   5.5 28 Black  Pin  (2 20.00  40.0) 1 Probe [2 13.99  24.2] 2 cb308.2
   1.0 28  Red   Pin  (2 13.00  09.0) 1 Probe [2 13.99  06.2] 1 cb311.1
   7.0 28  Red   Pin  (2 23.00  22.0) 1 Probe [2 13.99  06.2] 2 cb311.1
   1.0 28  Red   Pin  (2 13.00  10.0) 1 Probe [2 13.85  06.2] 1 cb305.1
   1.0 28  Red   Pin  (2 13.00  10.0) 2 Probe [2 13.85  06.2] 2 cb305.1
   5.0 28  Red   Pin  (2 20.00  01.0) 1 Probe [2 13.85  06.2] 3 cb305.1
   3.0 28 Black  Pin  (2 15.00  20.0) 1 Probe [2 13.99  03.5] 1 cb311.2
  10.0 28 Black  Pin  (2 19.00  60.0) 1 Probe [2 13.99  03.5] 2 cb311.2
   1.0 28 Black  Pin  (2 13.00  08.0) 2 Probe [2 13.85  03.5] 1 cb305.2
   1.0 28 Black  Pin  (2 13.00  08.0) 3 Probe [2 13.85  03.5] 2 cb305.2
   1.0 28  Blue  Pin  (2 15.11  41.0) 1 Probe [2 14.99  36.8] 1 u301.7
   2.5 28  Blue  Pin  (2 17.00  44.0) 1 Probe [2 14.85  36.8] 1 u301.6
   3.5 28  Blue  Pin  (2 19.00  42.0) 1 Probe [2 14.70  36.8] 1 u301.5
   3.5 28  Blue  Pin  (2 19.00  43.0) 1 Probe [2 14.56  36.8] 1 u301.4
   1.0 28  Blue  Pin  (2 14.00  42.0) 1 Probe [2 14.42  36.8] 1 u301.3
   1.0 28  Blue  Pin  (2 14.00  41.0) 1 Probe [2 14.27  36.8] 1 u301.2
   2.5 28  Blue  Pin  (2 17.00  42.0) 1 Probe [2 14.27  36.8] 2 u301.2
   2.0 28  Blue  Pin  (2 16.14  44.0) 1 Probe [2 14.99  34.8] 1 u301.10
   1.5 28  Blue  Pin  (2 15.11  42.0) 1 Probe [2 14.85  34.8] 1 u301.11
   2.0 28  Blue  Pin  (2 16.00  42.0) 1 Probe [2 14.70  34.8] 1 u301.12
   1.5 28  Blue  Pin  (2 15.00  43.0) 1 Probe [2 14.56  34.8] 1 u301.13
   1.5 28  Blue  Pin  (2 14.00  43.0) 1 Probe [2 14.42  34.8] 1 u301.14
   2.0 28  Blue  Pin  (2 14.00  44.0) 1 Probe [2 14.27  34.8] 1 u301.15
   1.5 28  Blue  Pin  (2 16.00  23.0) 1 Probe [2 14.99  29.5] 1 u302.7
   1.5 28  Blue  Pin  (2 15.00  22.0) 1 Probe [2 14.85  29.5] 1 u302.6
   1.5 28  Blue  Pin  (2 16.00  24.0) 1 Probe [2 14.70  29.5] 1 u302.5
   2.0 28  Blue  Pin  (2 16.00  22.0) 1 Probe [2 14.56  29.5] 1 u302.4
   1.0 28  Blue  Pin  (2 15.00  24.0) 1 Probe [2 14.42  29.5] 1 u302.3
   2.5 28  Blue  Pin  (2 16.00  21.0) 1 Probe [2 14.27  29.5] 1 u302.2
   4.5 28  Blue  Pin  (2 19.00  44.0) 1 Probe [2 14.13  29.5] 1 u302.1
   4.5 28  Blue  Pin  (2 18.00  51.0) 1 Probe [2 14.13  29.5] 2 u302.1
   3.0 28  Blue  Pin  (2 17.00  43.0) 1 Probe [2 14.99  27.5] 1 u302.14
   3.0 28  Blue  Pin  (2 16.00  43.0) 1 Probe [2 14.70  27.5] 1 u302.16
   1.0 28  Blue  Pin  (2 14.14  24.0) 1 Probe [2 14.27  27.5] 1 u302.19
   2.0 28  Blue  Pin  (2 16.99  23.0) 1 Probe [2 14.99  22.8] 1 u303.7
   4.5 28  Blue  Pin  (2 19.00  41.0) 1 Probe [2 14.56  22.8] 1 u303.4
   3.5 28  Blue  Pin  (2 15.00  02.0) 1 Probe [2 14.56  20.8] 1 u303.13
```

```
4.0 28  Blue  Pin  (2 19.00  04.0) 1 Probe [2 14.85  16.2] 1 u305.6
4.0 28  Blue  Pin  (2 19.00  03.0) 1 Probe [2 14.70  16.2] 1 u305.5
3.0 28  Blue  Pin  (2 16.00  02.0) 1 Probe [2 14.56  16.2] 1 u305.4
4.5 28  Blue  Pin  (2 17.00  41.0) 1 Probe [2 14.27  16.2] 1 u305.2
```

Figure 6-3 Fixture Wiring File

7 REFERENCE INFORMATION

The following sections define reference documents that are useful in clarifying the products or process of the industry or provide additional insight into the subject of data modeling or released information models.

7.1 IPC (1)

IPC-2221	Design Standard for Rigid Printed Boards and Rigid Printed Board Assemblies
IPC-D-300	Printed Board Dimensions and Tolerances
IPC-D-310	Guidelines for Artwork Generation and Measurement Techniques for Printed Circuits
IPC-D-325	Documentation Requirements for Printed Boards, Assemblies and Support Drawings

7.2 American National Standards Institute (2)

ANSI X3/TR-1-77	American National Dictionary for Information Processing
ANSI X3.12	Subroutine Record Format Standardization
ANSI Y14.5	Dimensioning and Tolerancing for Engineering Drawing
ANSI Y32.1	Logic Diagram Standards
ANSI Y32.16	Electrical and Electrical Reference Designators
ANSI Z210.1	Metric Practice Guide (ASTM 380-72)

7.3 Department of Defense (3)

DoD-STD-100	Engineering Drawings

7.4 Electronic Industries Association (4)

EDIF 4 0 0	Electronic Data Interchange Format

7.5 International Organization for Standards (ISO)

ISO STEP Documentation

AP210	Electronic Printed Circuit Assembly: Drawings and Manufacturing
AP211	Electronic PC Assembly, Test Diagnostics & Remanufacture
AP221	Process Plant Functional Data & Schematic Representation

Appendix A

EXPRESS defines data objects and their relationships among data objects for a domain of interests. Some typical applications of data models include supporting the development of databases and enabling the exchange of data for a particular area of interest. As an example, a specific requirement of a database for an audio compact disc (CD) collection is shown in Figure 1.

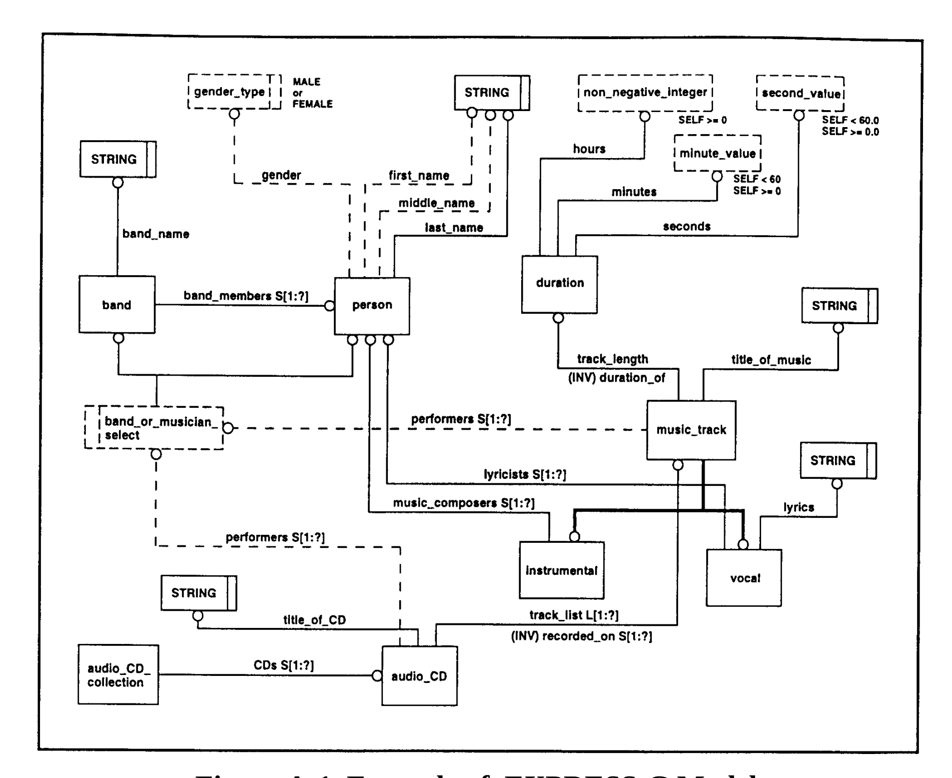


Figure A-1 Example of EXPRESS-G Model

Data models are specified in a data modeling language. EXPRESS is a data modeling language defined in ISO 10303-11. One of the advantages of using EXPRESS-G over EXPRESS is that the structure of a data model can be more intuitively presented. A disadvantage of EXPRESS-G is that complex constraints cannot be formally specified. There are specific symbols used in EXPRESS-G notation. The meaning of those symbols is defined in the EXPRESS formatting.